Memristive Circuits and Architectures for Neuro-Inspired Computing
Dr. Garrett S. Rose

Abstract:
For over four decades silicon-based CMOS has been the core technology that has continued to enable
great advances in computer systems that have become commonplace in modern society. While CMOS
scaling is still pushing further into the nanometer regime, now reaching 14 nm gate lengths, it is also
true that fundamental limits to such scaling are fast approaching. Thus, several novel nanoelectronic
devices have emerged in recent years as potential candidates for “beyond CMOS” technology. At the
same time, new approaches to computer architecture design, including neuromorphic computing, are
being considered for a multitude of contemporary challenges and emerging applications. The focus of
this talk is the utilization of memristors and memristive systems, a novel “beyond CMOS” device
technology family, in the construction of novel, neuro-inspired circuits and architectures. In all of the
implementations considered here, memristors are used as artificial synapses – a natural fit given the
property of hysteretic switching that defines memristors. We begin by considering basic threshold logic
where memristors are used to represent the weights in a perceptron circuit that can be trained to
perform a wide variety of possible functions. Results using a stochastic gradient descent method for
training memristive threshold logic circuits will also be discussed. Finally, hardware implementations
of the “Brain-State-in-a-Box” (BSB) algorithm, including both recall and training, will be presented.
While specific algorithms are considered here, many of the fundamental building blocks can be applied
to a wide variety of possible neuro-inspired architectures. It is expected that the realization of such
architectures will improve the performance and efficiency of many existing and emerging applications.

Bio:
Garrett S. Rose received the B.S. degree in computer engineering from Virginia Tech in 2001 and the
M.S. and Ph.D. degrees in electrical engineering from the University of Virginia in 2003 and 2006,
respectively. Presently, he is an Associate Professor in the Department of Electrical Engineering and
Computer Science at the University of Tennessee, Knoxville where his work is focused on research in
the areas of nanoelectronic circuit design, neuromorphic computing and hardware security. Prior to
joining UTK, from June 2011 to July 2014, he was with the Air Force Research Laboratory (AFRL),
Information Directorate, Rome, NY. While with AFRL, he worked as a Senior Electronics Engineer in
the Trusted Systems Branch concentrating on research in chaos computing, memristor-based
neuromorphic hardware design and the implementation of hardware security primitives from
nano electronic devices. From August 2006 to May 2011, he was an Assistant Professor in the
Department of Electrical and Computer Engineering at the Polytechnic Institute of New York
University, Brooklyn, NY. He is a member of the Association of Computing Machinery, IEEE Circuits
and Systems Society and IEEE Computer Society. He serves and has served on Technical Program
Committees for several IEEE conferences (including ISCAS, GLSVLSI, NANOARCH) and
workshops in the area of VLSI design. In 2010, he was a guest editor for a special issue of the ACM
Journal of Emerging Technologies in Computing Systems that presented key papers from the
he is an associate editor for IEEE Transactions on Nanotechnology.